REMARKS/ARGUMENTS

Applicants have received the Office Action dated February 7, 2007, in which the Examiner: 1) rejected claims 1-2, 6-7, 13-14, 19, 22, and 24 as indefinite over 35 U.S.C. § 112, second paragraph, 2) rejected claims 1-5, 7-9, 13-15, 19-20, and 22-24 under 35 U.S.C. § 103 as being unpatentable over Witt et al (U.S. Pat. No. 6,256,728, hereinafter "Witt") in view of Chudnovsky et al. (U.S. Pat. No. 6,381,669, hereinafter "Chudnovsky"), 3) rejected claims 6 and 21 under 35 U.S.C. § 103 as being unpatentable over Witt in view of Chudnovsky and further in view of Rowlands et al. (U.S. Pat. No. 6,748,492).

With this Response, Applicants have amended claims 1-2, 6-8, 13-14, 19, 22, and 24.

I. SECTION 112, ¶ 2 REJECTIONS

The Examiner has issued various § 112, ¶ 2 rejections over language suggesting a relative nature, such as "fast," "faster," and "shorter." Applicants disagree with the Examiner that such terms are indefinite in light of the specification describing the claimed first way, but have amended each of these claims in order to advance prosecution.

The Examiner has also rejected claims 1, 7, and 22 as omitting essential elements to accomplish "a faster access time." Applicants disagree with the Examiner that the claims are indefinite in light of the specification describing the claimed first way having an access time faster than that of other ways based on its physical proximity to the access control logic, but have amended each of these claims in order to advance prosecution.

Additionally, Applicants have amended claim 6 to address the Examiner's concerns with regard to the claim term "proper control." Claim 6 has also been amended to include the control signals that control the muxes from the access control logic.

For at least these reasons, Applicants respectfully request withdrawal of the rejections over § 112, ¶ 2.

II. SECTION 103 REJECTIONS

To summarize, the Examiner asserts that each claim limitation of the pending claims may be found either in the combination of Witt and Chudnovsky or the combination of Witt, Chudnovsky and Rowlands. The Applicants disagree, however, with the reading of some of the art by the Examiner.

To clarify, Witt discloses a process configured to selectively cancel instructions from its pipeline based on predictive processing. The disclosure of Witt discloses various caches and various control units. It is not clear to the Applicants how the Examiner finds the claimed limitations present in Witt. For example, the set associative cache pointed to by the Examiner (col. 12, lines 36-44) is not coupled to the fetch control unit 18, which Examiner asserts is analogous to the access control unit as claimed. Likewise, the muxes to which the Examiner directs the Applicants' attention are within the instruction queue, not the architecture of the cache itself as claimed in the present application. Furthermore, the Examiner points to faster access times as to between different caches (col. 8, lines 30-37), while the present disclosure references the access time to various ways within a single cache. Applicants respectfully assert that each of the claims are in condition for allowance over Witt, as discussed in greater detail below.

As amended, Claim 1 requires "access control logic which manages access to the cache and is coupled to said plurality of ways, the access control logic being physically closer to the first way than to the other ways of the plurality of ways; a plurality of muxes coupled to said first way in each of said banks and coupled to said access control logic; and wherein the access control logic controls the mux in a bank to remap any defective way in a bank to the first way in that same bank." Neither Witt, as discussed above, nor Chudnovsky, disclose access control logic which is coupled to a plurality of ways, wherein the access control logic controls the mux to remap any defective way to the first way in the same bank that is physically closer to the access control logic than the other ways.

While Witt discloses in passing a set associative cache, it is unclear to the Applicants that any other claim limitation is found in Witt. While similar language or terminology may be used in the disclosure of Witt, such language is not

directed to characteristics or features of the set associative cache itself, as claimed.

Chudnovsky specifically discloses a scrambling addressing technique that reduces the number of faults in a chip, but nowhere discusses remapping a defective way to a specific first way with faster access time based on close proximity to the access control logic. Chudnovsky does disclose storing a list of defective banks in memory, but remapping of Chudnovsky is based on a scrambling algorithm to achieve addressing that is at least somewhat random. For at least these reasons, claim 1 and the claims depending therefrom are believed to be in condition for allowance. Claims 13, 19, and 24 are rejected based on substantially similar reasoning as claim 1. For at least the same reasons, claims 13, 19, and 24 and the claims depending therefrom, are believed to be in condition for allowance as well.

With regard to claim 6, the reasoning discussed above with respect to claim 1 applies, and Rowlands further lacks the same claim limitations. Rowlands discloses storing in a register the tag information of a way (from a plurality of ways) selected, based on a replacement policy, to be evicted to make room for more often used data. (*See* Rowlands, Col. 1, lines 49-52, Col. 2, lines 50-60, Col. 11, lines 3-32). Thus, Rowlands also lacks an access control logic coupled to the ways, that, using a mux, remaps any defective way in a bank to the first way, wherein the first way has a faster access time than the access time of the other ways. For at least this reason, claim 6 is also believed to be in condition for allowance.

With regard to claim 21, the reasoning discussed above with respect to claim 19 applies. Furthermore, Rowlands lacks the same claim limitations as discussed above with respect to Witt and Chudnovsky, and the Applicants disagree with the assertion of the Examiner that Rowlands contains the additional claim limitation added by claim 21. Specifically, the Examiner asserts that Rowlands discloses disabling a way in a bank when the way is defective. However, Rowlands clearly indicates that when a way is evicted, the eviction is to make room for newly access data that is more likely to be accessed again in the

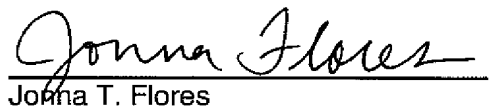
near future than the data that it replaces, clearly indicating that the way will continue to be used. (*See* Rowland, Col. 1, lines 30-35). By contrast, claim 21 requires that a way that is defective be disabled, instead of continuing to be used since the data stored in a defective way is unreliable. For at least this reason, claim 21 is also believed to be in condition for allowance.

III. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



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